

REMARKS/ARGUMENTS

Claims 1-6 are rejected under 35 U.S.C. 102(e) as being anticipated by Chuang et al. (U.S. 20030096486 A1). Claims 7-27 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-5 of Chen (U.S. Patent No. 6,759,731 B2) in view of Chuang et al. (U.S. 20030096486 A1).

1. Rejection of claims 1-6 over 35 U.S.C. 102(e):

Claims 1-6 are rejected under 35 U.S.C. 102(e) as being anticipated by Chuang et al. (U.S. 20030096486 A1). Chuang discloses a self-aligned bipolar transistor with

- (claim 1) a substrate (202);
- a dielectric layer (204, 206) formed on the substrate (202);
- an opening (208) formed in the dielectric layer (204, 206) to expose a portion of the substrate (202) (see Figures 2A-2B);
- a semiconductor layer (212) formed on a sidewall and a bottom of the dielectric layer (208), the semiconductor layer (212) extending outside the opening (208) and above the dielectric layer (204, 206) (see Figures 2A-2D);
- a spacer (210) formed on the semiconductor layer (212) to define a self-aligned emitter region in the opening (208);
- an emitter conductivity layer (212a) being filled into the self-aligned emitter region, and a PN junction being formed between the emitter conductivity layer (212a) and the semiconductor layer (212) (see Figures 2A-2E);
- a salicide layer (222) formed on the emitter conductivity layer (212a) and on the portion of the semiconductor layer (212) extending outside the opening (208) and above the dielectric layer (204, 206) (see Figures 2A-2H);

(claim 2) wherein the semiconductor layer comprises at least one material selected from a material group consisting of silicon epitaxy, GaAs, InP and AlGaAs (see

paragraph [0047]);

(claim 3) further comprising a selective implant collector region formed in the substrate beneath the semiconductor layer (see Figures 2A-2H);

(claim 4) further comprising an extended conductivity layer formed on the dielectric layer to connect to the semiconductor layer (see Figures 2A-2H);

(claim 5) further comprising an oxide layer and a silicon nitride layer formed between the extended conductivity layer and the dielectric layer (see Figures 2A-2H);

(claim 6) wherein the extended conductivity layer is composed of polysilicon (see Figures 2A-2H).

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Response:

With reference to Figs.12-14 of this application, claim 1 is listed as below for explaining the difference of this application between the cited application:

“Claim 1: A bipolar junction transistor, comprising:

15 a substrate (P-type semiconductor substrate 70);

a dielectric layer (84) formed on the substrate (70);

an opening (98) formed in the dielectric layer (84) to expose a portion of the substrate;

20 a semiconductor layer (103) formed on a sidewall and a bottom of the opening (98), the semiconductor layer (103) extending outside the opening and above the dielectric layer (84)(see para. [0028]);

a spacer (106) formed on the semiconductor layer (103) to define a self-aligned emitter region in the opening (98);

25 an emitter conductivity layer (108) being filled into the self-aligned emitter region, and a PN junction being formed between the emitter conductivity layer and the semiconductor layer; and

a salicide layer (110) formed on the emitter conductivity layer (108) and on the portion of the semiconductor layer (103) extending outside the opening and above the

dielectric layer.”

As a result, claim 1 limits that *the semiconductor layer 103 (referring to Fig.14) is formed on the sidewall and the bottom of the opening 98 and extending outside the opening 98, and a salicide (metal silicide) 110 is formed on the surface of the portion of the semiconductor layer 103 outside the opening 98.* In addition, since the spacer 106 is only formed on the inside sidewall of the opening 98 but not formed on the bottom surface of the opening 98, *the emitter conductivity layer 108, which is filled in the self-aligned emitter region defined by the spacer 106, directly contacts the semiconductor layer 103 on the bottom surface of the opening 98.* As a result, *a PN junction is formed between the interface between the semiconductor 103 and the emitter conductivity layer 108.*

Referring to Figs.2A-2H of the application of Chuang et al., a bipolar transistor is disclosed, which has a substrate 200, a base 202 formed by an eptiaxial layer or silicon germanium (para. [0033], line 3) disposed on the substrate 200, and an insulating layer 204 and a conductive material 210 forming an opening on the base 202. According to the fabrication method of Chuang et al., a conductive layer 212 is filled in the opening (Figs.2D-2E) before performing a first conductive type doping 214 for forming the emitter 212a. Then, portions of the insulating layer 204 are removed, and a second conductive type doping 216 is performed to form the extrinsic base contact region 218 in the base (epitaxial layer) 202 (Fig.2G). Sequentially, the spacer 220 is formed on outside sidewalls of the insulating layer 204 and the conductive layer 210. Finally, a self-aligned silicide process is performed to form the salicide 222 on the surfaces of the emitter 212a and the extrinsic base contact region 218.

Accordingly, in the bipolar transistor disclosed by Chuang et al. in Figs. 2A-2H, *only the base 202 could be considered as a semiconductor layer because the emitter 212a,*

the conductive layer 210, and the extrinsic base contact region 218 are all conductive. However, the base 202 is not positioned in the opening formed by the insulating layer 204, while there are only the emitter 212a formed in the opening. In fact, there is no insulating material formed next to the base 202. In addition, the base 202 never extends outside the opening, but is surrounded by the extrinsic base contact region 218, without any silicide or silicide materials formed on its surface.

Furthermore, the Examiner points that the emitter 212a of Chuang et al. is filled into the self-aligned emitter region and a PN junction is formed between the emitter 212a and the semiconductor 212. However, according to Figs. 2D to 2E, *the emitter 212a is formed from the conductive layer 212*, wherein a portion of the conductive layer 212 is removed by an etching back or a CMP process to form the emitter 212a (para. [0037]-[0038]). *Therefore, obviously, the conductive 212 formed with polysilicon material is not a semiconductor layer, and there would never occur a PN junction between the emitter 212a and the conductive layer 212 since the emitter 212a is a part of the conductive layer 212.* To make short of the matter, *Chuang et al. never disclose the arrangement or relative position of the semiconductor layer and other elements nor teach forming silicide materials on the surface of the semiconductor layer (In contrast, the silicide layer 222 of Chuang et al. is formed on the conductive extrinsic base contact region 218), limited by claim 1 of this application.* As a result, the bipolar transistor disclosed by Chuang et al. is quite different from the bipolar junction transistor described in claim 1 of this application. Applicant believes that claim 1 should be allowable, thus reconsideration of claim 1 is politely requested.

Regarding to claim 2 of this application, it describes that the **semiconductor layer 103** comprises at least one material selected from a material group consisting of silicon epitaxy, GaAs, InP and AlGaAs. Examiner considers that para. [0047] of the cited prior art has disclosed the content of claim 2. However, in fact, it is the **semiconductor**

substrate 200 can be formed by GaAs, SiGe, InP in para. [0047] of Chuang et al, *not the conductive layer (base) 212*. It could be easily realized that the semiconductor substrate 200 is apparently not the semiconductor layer mentioned in claim 2 of this application when considering the whole structure and functionality of the two elements. On the other
5 hand, the base 212 comprising polysilicon (para. [0037], line 3) which composes the emitter 212a is not a semiconductor layer at all. Since Chuang et al. never teach that the conductive layer 212 may be replaced by semiconductor materials nor suggest to use the above-mentioned materials to form the conductive layer 212, claim 2 of this application is never disclosed by the cited prior art and should be patentable according to 35 U.S.C.
10 102(e). Accordingly, reconsideration of claim 2 is respectfully requested.

With reference to claim 3 of this application, it defines the bipolar junction transistor further comprises *a selective implant collector region 102 formed in the substrate 70 beneath the semiconductor layer 103 (Figs.12-14)*. However, Chuang et al. never teach
15 forming any selective implant collector regions in the substrate 200 or the base 202. In fact, *there is no implant collector region disposed inside the substrate 200 of the cited application*. Therefore, Chuang et al. do not disclose the content of claim 3 of this application, and claim 3 should be allowable. Reconsideration of claim 3 is thereby requested.

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Regarding to claim 4, it describes that an extended conductivity layer 96 is formed on the dielectric layer 84 and connecting to the semiconductor layer 103. *The conductive layer 210 in Fig.2H of Chuang et al. could be considered as an extended conductivity layer, but it never connects to the base 202 with the semiconductor material*. Accordingly,
25 Chuang et al. never disclose the limitation of claim 4 of this application. Applicant believes claim 4 should be allowable, and reconsideration of claim 4 is politely requested.

Regarding to claim 5, it limits that the bipolar junction transistor further comprises

an oxide layer 92 and a silicon nitride layer 94 formed between the extended conductivity layer 96 and the dielectric layer 84 (Fig.14). However, *according to the figures, Chuang et al. does not teach forming any oxide layer or silicon nitride layer in their structure.* Therefore, claim 5 of this application should be allowable. Reconsideration of claim 5 is respectfully requested.

Regarding to claim 6, since claim 6 is dependent upon claims 1 and 4, it should be allowable if claims 1 and 4 are allowable. Reconsideration of claim 6 is hereby requested.

2. Rejection of claims 7-27:

Claims 7-27 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-5 of Chen (U.S. Patent No. 6,759,731 B2) in view of Chuang et al. (U.S. 20030096486 A1), as cited on pages 4-5 of the above-identified Office action.

Response:

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) is proposed, which is accompanied with this paper, for overcoming this rejection. Acceptance of the terminal disclaimer and allowable of claims 7-27 are politely requested.

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Appl. No. 10/709,568
Amdt. dated June 07, 2007
Reply to Office action of April 19, 2007

Sincerely yours,

Winston Hsu

Date: 06.07.2007

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- 10 Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 12 hours behind the Taiwan time, i.e. 9 AM in D.C. = 9 PM in Taiwan.)